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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,954	AIGO, TAKAO	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 3/8/2007.

2. Claims 1, 3-4, 6, 8-9, 11, and 14 have been amended.

3. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Objections

4. Claims 1-2 objected to because of the following informalities:

a. In line 10 of claim 10, the phrase, "the high priority tasks" does not have antecedent basis. Was the intention to say, "the first priority tasks" in accordance with the other independent claims?

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil et al., US patent 6085287, Niitaka, et al., EP 0400500, and Williams, US patent application publication 2001/0042090.

8. With respect to claims 1 and 6, O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57); and

wherein said second element adjusts a number of activated ones of the according to the calculated cache hit ratio (fig. 2; item 28; column 4, lines 34-39).

O'Neil fails to specifically teach of a second element constructed and arranged so that the second element executes tasks as a first priority unless a number of the first priority tasks in execution exceeds a first number, and executes one of the tasks as a second priority when the number of the first priority tasks in execution exceeds the first number, wherein the first priority is higher than the second priority.

However, Niitaka teaches of a second element constructed and arranged so that the second element executes tasks as a first priority unless a number of the tasks executed as the first priority exceeds a first number, and executes one of the tasks as a second priority when the number of the tasks executed as the first priority exceeds the

first number, wherein the first priority is higher than the second priority (column 2, line 46-column 3, line 12).

The combination of O'Neil and Niitaka fails to specifically teach of the number of first priority tasks *in execution* exceeding a first number. However, Williams teaches of executing prioritized tasks concurrently and limiting the number of concurrently executed tasks to a specified number (paragraph 15).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil and Niitaka at the time of the invention to execute second priority tasks when a number of first priority tasks are executing. Their motivation would have been to ensure low priority tasks are executed within a reasonable time (Niitaka, abstract).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil, Niitaka, and Williams at the time of the invention to concurrently execute the tasks of the combination of O'Neil and Niiaka as taught in Williams. Their motivation would have been to enable more efficient processing and increase system performance in the face of a heavy schedule load (Williams, paragraph 4).

9. Claims 2 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil, Niitaka, and Williams in further view of Bala US patent 6351844.

10. With respect to claims 2 and 7, the combination of O'Neil, Niitaka, and Williams fails to specifically teach of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value.

However, Bala teaches of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value (column 8, lines 34-46; if the cache hit rate is high, the threshold is raised so no more traces are examined (lower number of tasks). If it is low, the threshold is lowered so that an increasing number of traces are examined (higher number of tasks). Since the cache hit rate being high or low is used to vary the threshold, there must be a cache hit rate threshold that signifies a high or a low cache hit rate).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil, Niitaka, Williams, and Bala at the time of the invention to implement the cache system identifying hot traces of Bala in the cache memory system of the combination of O'Neil, Niitaka, and Williams. Their motivation would have been to efficiently identify the hot traces to capture the current working set in the cache memory (Bala, column 8, lines 38-40).

11. Claims 2-4, 7-9, 11, 13, 14, 16 rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil, Niitaka, Williams and Ryan US patent 5367656.

12. With respect to claims 2 and 7, the combination of O'Neil, Niitaka, and Williams fails to specifically teach of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and increases when the calculated cache hit ratio is below the prescribed value.

However, Ryan teaches of wherein the number of activated ones of the tasks decreases when the calculated cache hit ratio is above a prescribed value and

increases when the calculated cache hit ratio is below the prescribed value (fig. 1, 5; column 8, lines 63-column 9, line 7).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil, Niitaka, Williams, and Ryan at the time of the invention to include the cache predictive prefetching system of Ryan in the cache memory system of the combination of O'Neil, Niitaka, and Williams. Their motivation would have been to lower the cache miss ratio (Ryan, column 2, lines 40-42).

13. With respect to claims 3 and 8, Ryan teaches of a first element constructed and arranged so that the first element calculates a cache hit ratio at a cache memory (fig. 1, 5; column 2, lines 58-63);

wherein said second element executes only the first priority tasks when the cache hit ratio is above a prescribed value and executes both the first priority tasks and second priority tasks when the cache hit ratio is below the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs and regular cache accessing occurs. The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are high priority tasks since they are required for processor to carry out the program. The miss prediction is a low priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out).

O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

Niitaka teaches of a second element which executes tasks as a first priority unless a number of the first priority tasks executed as the first priority exceeds a first number, and executes one of the tasks as a second priority when the number of the first priority tasks executed exceeds the first number, wherein the first priority is higher than the second priority (column 2, line 46-column 3, line 12).

Williams teaches of executing prioritized tasks concurrently and limiting the number of concurrently executed tasks to a specified number (paragraph 15).

14. With respect to claim 4, Ryan teaches of a cache hit determination unit constructed and arranged to determine whether or not the I/O process request is causing a cache hit at a cache memory (fig. 2; column 4, lines 7-14);

a cache hit ratio monitor unit constructed and arranged to calculate and output a cache hit ratio within some period of time by using a determination result of the cache hit determination unit (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio, the hit ratio must be calculated based on wither the requests were hits or misses in the cache memory); and

an execution task selection unit constructed and arranged to assign each said I/O process request to either the first or second priority tasks (fig. 1, 3-5; column 4, lines 7-14; upon the operand/data request, the request are sent to determine if they result in a cache hit or miss (first priority I/O)),.

the execution task selection unit assigning said I/O process request to the first priority tasks when the cache hit ratio is not less than some prescribed value and assigning said I/O process request to the second priority tasks when the cache hit ratio is less than the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs (second priority) and regular cache accessing occurs (first priority). The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are first priority tasks since they are required for processor to carry out the program. The miss prediction is a second priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out (first priority I/O execution unit)).

O'Neil teaches of a disk array control apparatus comprising: a host I/O reception unit arranged so that the host I/O reception unit receives as an input an I/O process request from a host computer, the I/O reception unit generating as an output the I/O process request (fig. 2; item 22, column 3, lines 54-65) and a disk cache memory (fig. 2; item 18).

Niitaka teaches of an I/O process execution unit that executes tasks as a first priority unless a number of the first priority tasks executed exceeds a first number, and executes one of the tasks as a second priority when the number of the first priority tasks

executed exceeds the first number, wherein the first priority is higher than the second priority (column 2, line 46-column 3, line 12).

an execution task selection unit constructed and arranged to assign each said I/O process request to either the first or second priority tasks (column 2, lines 46-48).

Williams teaches of executing prioritized tasks concurrently and limiting the number of concurrently executed tasks to a specified number (paragraph 15).

15. With respect to claim 9, Ryan teaches of a control method comprising the steps of: inputting an I/O process request from a host computer (fig. 2; column 4, lines 7-10);

determining whether the I/O process request is causing a cache hit at a cache memory (fig. 2; column 4, lines 7-14);

calculating a cache hit ratio within some period of time based on results of the determining step (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio of such, the hit ratio must be calculated based on wither the requests were hits or misses in the cache memory);

assigning the I/O process request to the first priority tasks when the cache hit ratio is not less than some prescribed value; and assigning the I/O process request to the second tasks and low priority tasks when the cache hit ratio is less than the prescribed value (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs and regular cache accessing occurs. The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are first priority tasks since they are required for

processor to carry out the program. The miss prediction is a second priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out).

O'Neil teaches of a disk array control method comprising: calculating a cache hit ratio within some period of time at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

Niitaka teaches of an executing tasks as a first priority unless a number of the first priority tasks executed exceeds a first number, and executing one of the tasks as a second priority when the number of the first priority tasks executed exceeds the first number, wherein the first priority is higher than the second priority (column 2, line 46-column 3, line 12).

Williams teaches of executing prioritized tasks concurrently and limiting the number of concurrently executed tasks to a specified number (paragraph 15).

16. With respect to claims 11 and 14, the combination of Ryan, O'Neil, Niitaka, and Williams teach of the limitations of the claims as previously described.

17. With respect to claims 13 and 16, O'Neil teaches of a disk cache memory which is accessed by one of the first or second priority tasks; and a plurality of disks which are accessed by said one of the first or second priority tasks when said disk cache memory does not have data for said one of the first or second priority tasks (fig. 2; column 3, lines 39-53; as taught in the combination, the different commands are of the different priorities).

18. Claims 5, 10, 12, 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan, O'Neil, Niitaka, and Williams as applied to claims 4, 9, 11, 14 respectively, and further in view of Horii et al., JP 08-077025 A.

19. With respect to claims 5, 10, 12, 15 the combination of Ryan, O'Neil, Niitaka, and Williams fails to specifically teach of a task priority change unit constructed and arranged to dynamically change the second priority task to one of the first priority tasks after starting execution of the second priority task, the task priority change unit changing the one of the first priority tasks whose priority has been changed to the first priority back to the second priority tasks at execution termination time.

However, Horii teaches of a task priority change unit constructed and arranged to dynamically change the second priority task to one of the first priority tasks after starting execution of the second priority task, the task priority change unit changing the one of the first priority tasks whose priority has been changed to the first priority back to the second priority tasks at execution termination time (paragraph 0009).

It would have been obvious to one of ordinary skill in the art having the teachings of Ryan O'Neil, Niitaka, Williams, and Horii at the time of the invention to modify the priority of the tasks while they are being executed as taught in Horii. Their motivation would have been to avoid the inversion phenomenon of priority, where a low priority task is executed before a high priority task (Horii, paragraph 0005).

Response to Arguments

20. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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